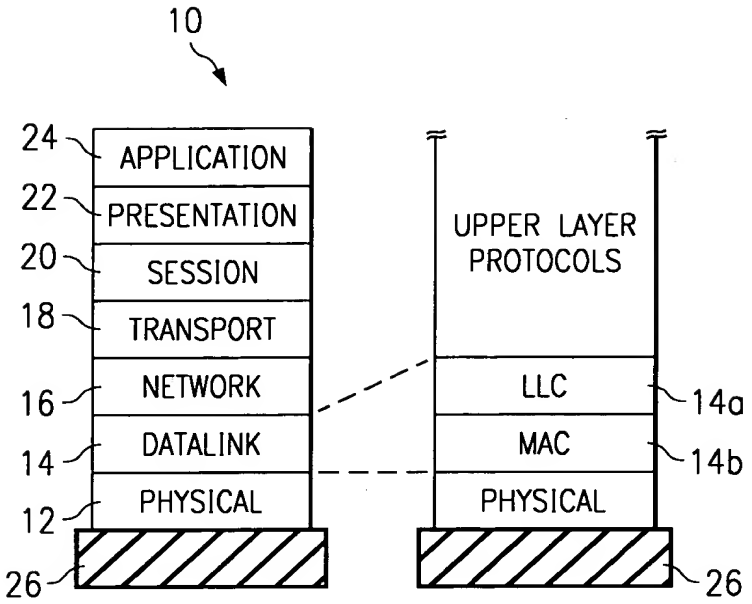

FIG. 1

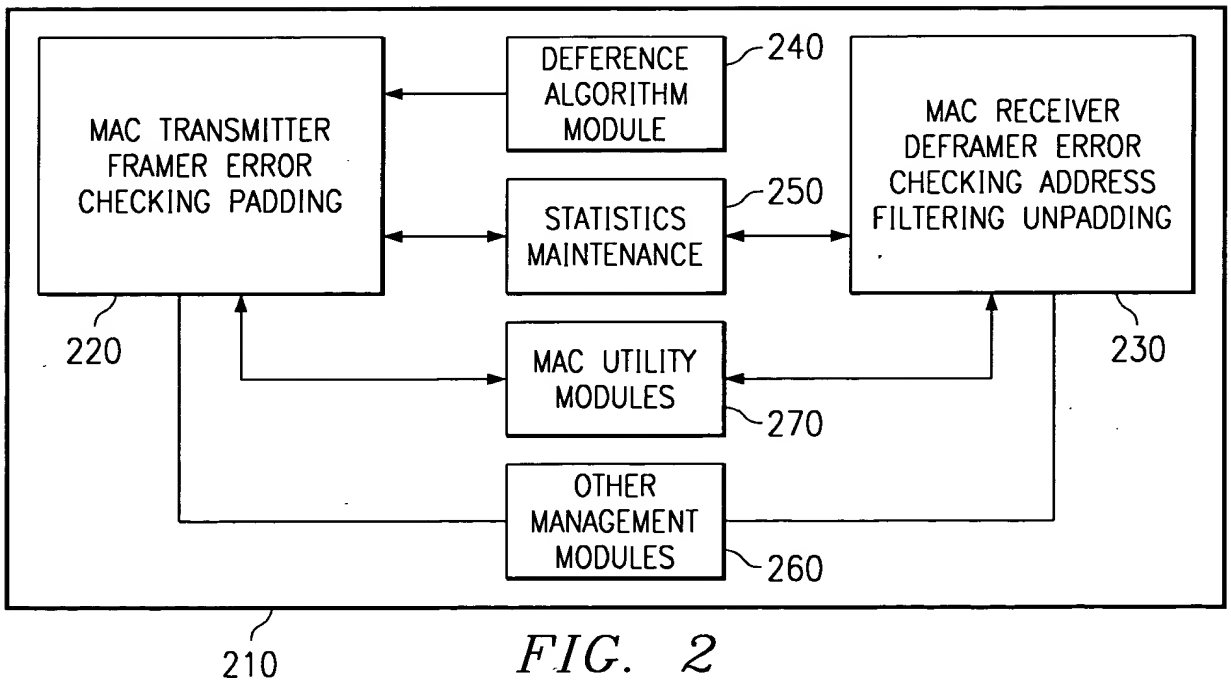

FIG. 2

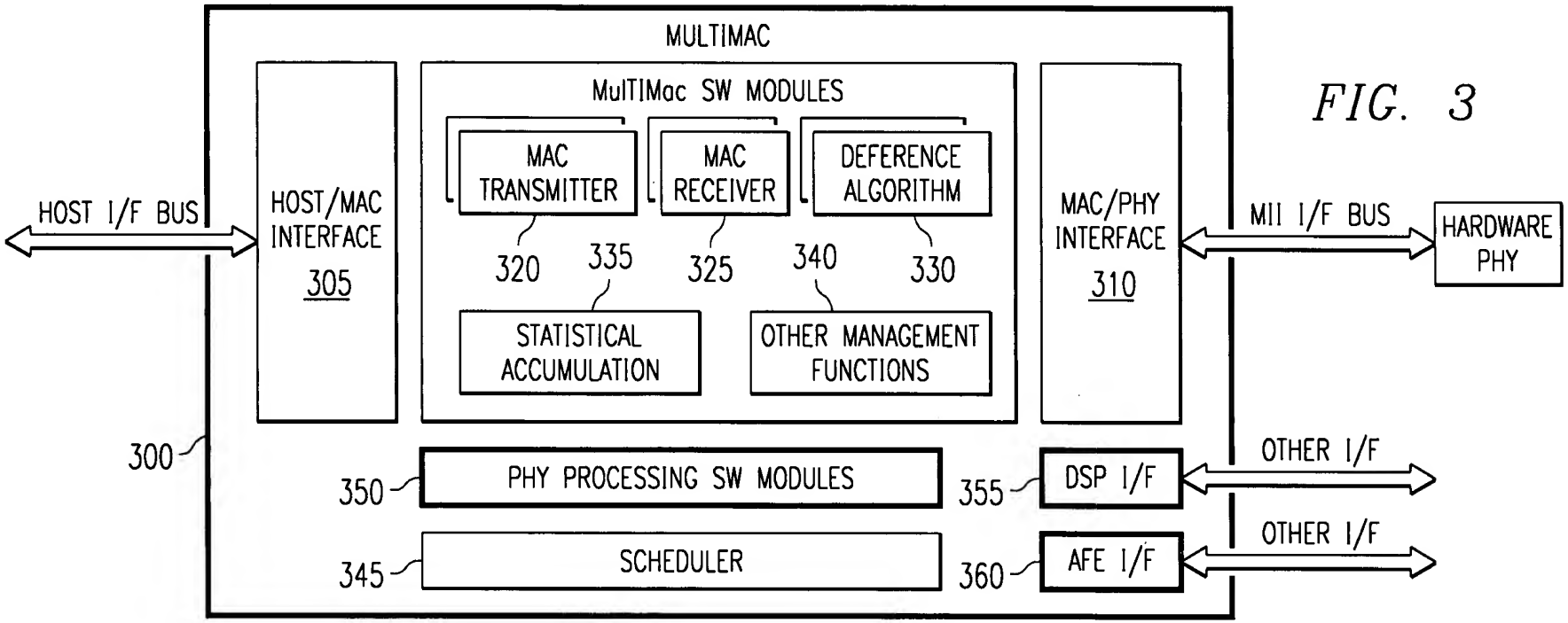

FIG. 3

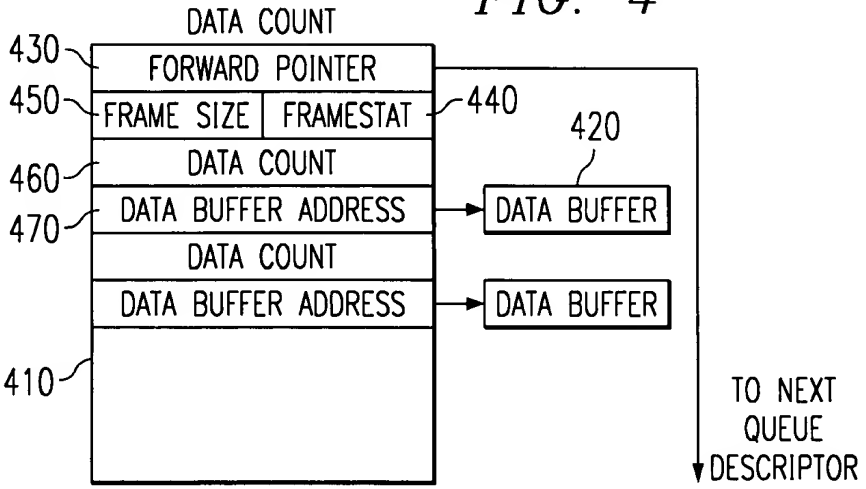

FIG. 4

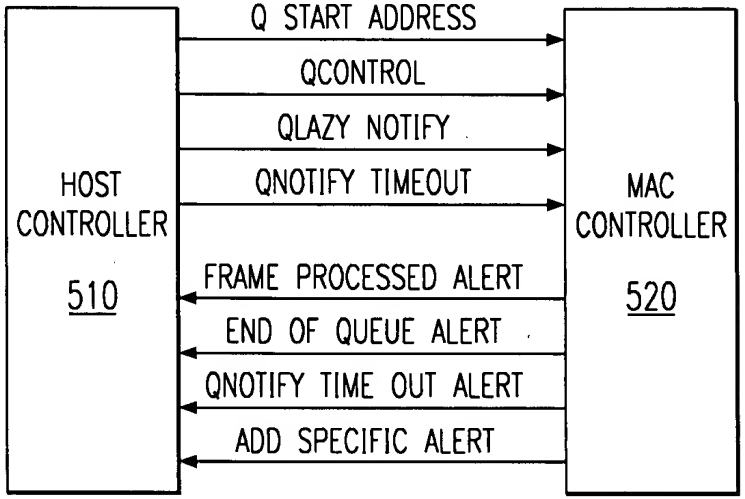

FIG. 5

S/N: 09/737,714
FORMAL DRAWINGS

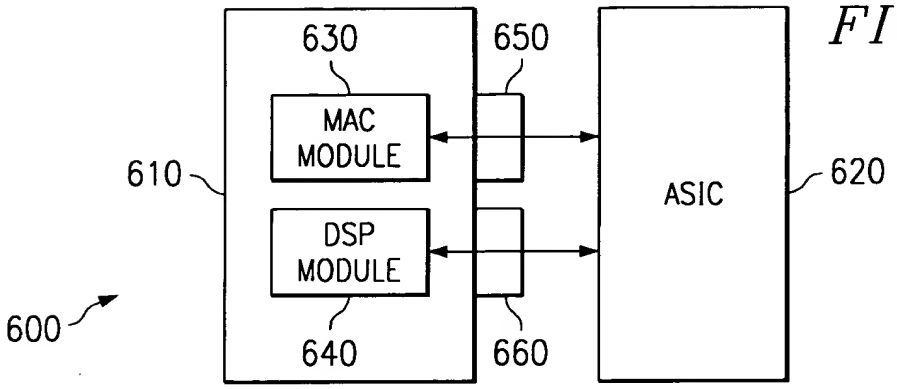

FIG. 6

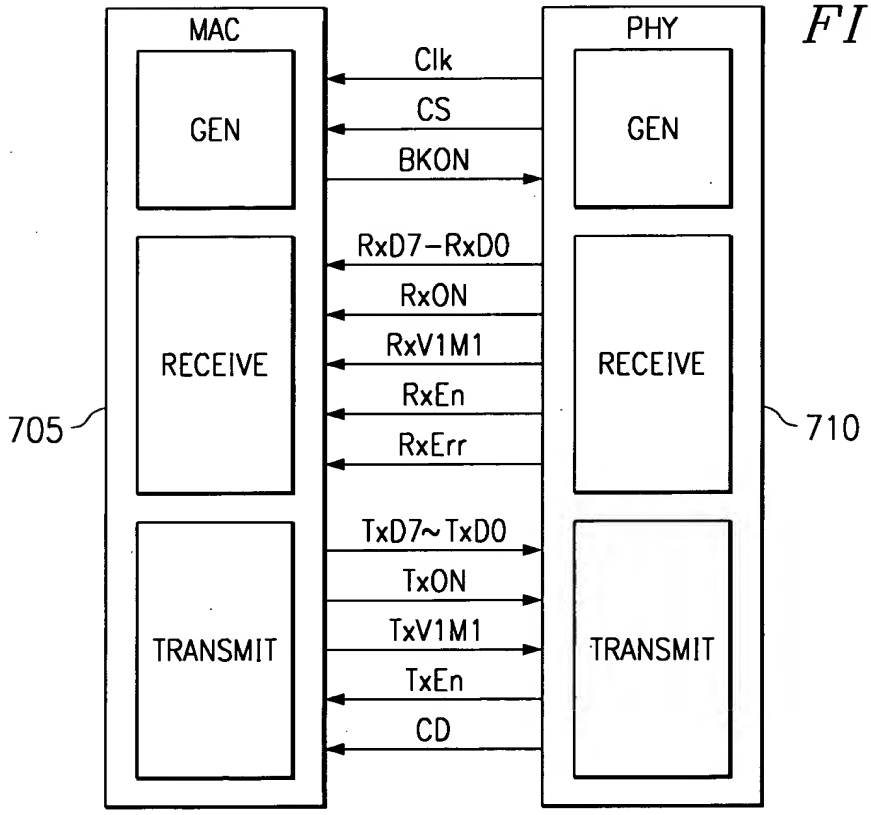

FIG. 7

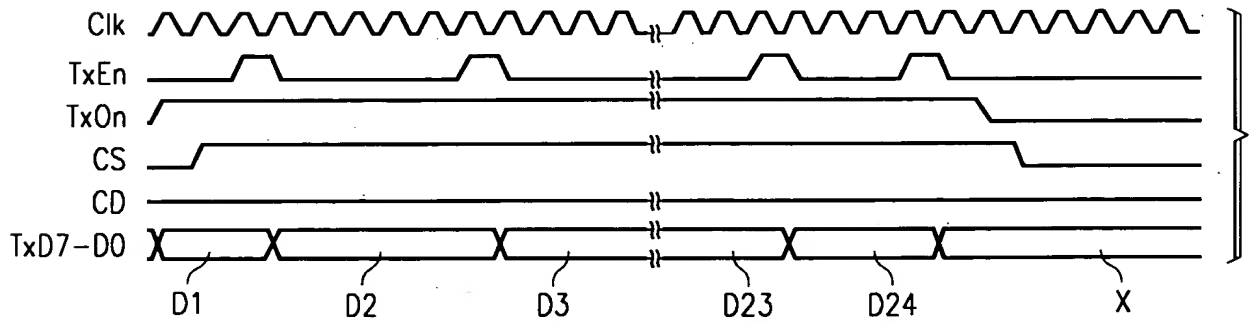

FIG. 8

FIG. 9

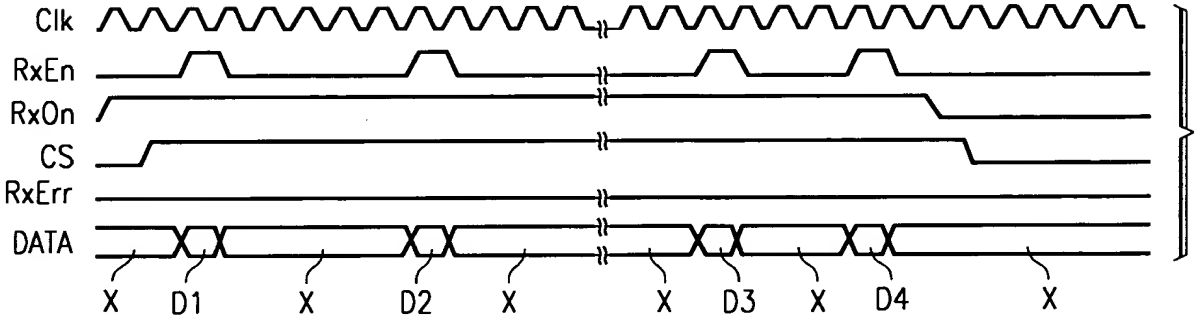

FIG. 10

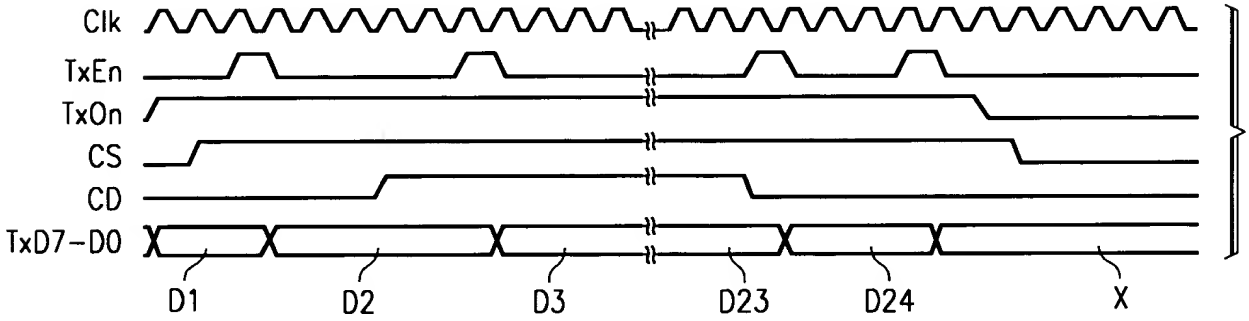

FIG. 11

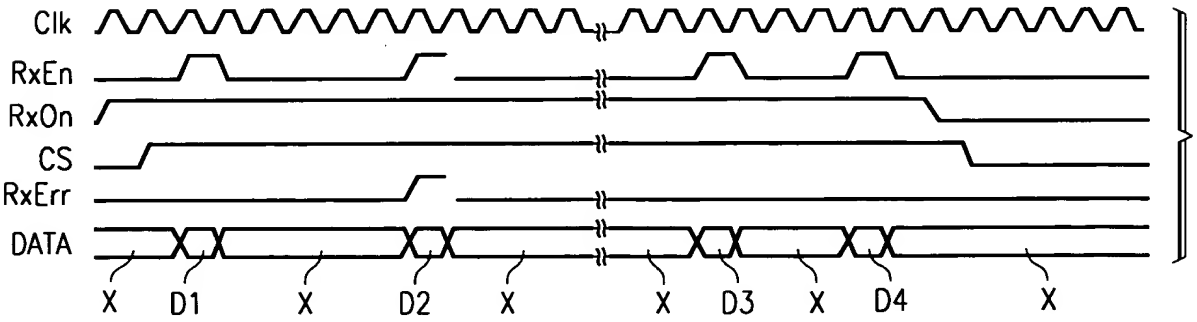

FIG. 12

REGISTER ADDRESS	REGISTER NAME	DESCRIPTION	R/W	IMPLEMENTATION
0	Tx ADDRESS REGISTER	TxFRAME START ADDRESS	MAC WRITE	MAC
1	Tx LENGTH REGISTER	TxFRAME LENGTH	MAC WRITE	PHY
2	Rx ADDRESS REGISTER	RxFRAME START ADDRESS	MAC WRITE	MAC
3	Rx LENGTH REGISTER	RxFRAME LENGTH	MAC READ	PHY
4	CONTROL REGISTER	FRAME TRANSMIT AND RECEIVE CONTROL REGISTER	MAC WRITE	MAC
5	STATUS REGISTER	PHY SIGNALING STATUS	MAC READ	MAC
6	INTERRUPT MASK REGISTER	PHY TO MAC INTERRUPT MASKS	MAC WRITE	MAC
7	INTERRUPT STATUS REGISTER	INTERRUPT STATUS	MAC READ	MAC
8	CRC32 HIGH REGISTER	CRC32 HIGH 16 BITS	MAC READ	PHY
9	CRC32 LOW REGISTER	CRC32 LOW 16 BITS	MAC READ	PHY
10	CRC16 REGISTER	CRC16	MAC READ	PHY
11	PHY MANAGEMENT CONTROL REGISTER	DESCRIBED IN 5	HOST/MAC WRITE	PHY
12	PHY MANAGEMENT STATUS REGISTER	DESCRIBED IN 5	HOST/MAC READ	PHY

FIG. 13

BITS	NAME	DESCRIPTION	R/W
15	TxON	1=SET TxON SIGNAL 0=CLEAR TxON SIGNAL	R/W
14	BkON	1=SET BkON SIGNAL 0=CLEAR BkON SIGNAL	R/W
13	TxV1M1	1=SET TxV1M1 SIGNAL 0=CLEAR TxV1M1 SIGNAL	R/W
12~8	RESERVED	WRITE AS 0, IGNORE ON READ	R/W
7	INTERRUPT ENABLE	1=PHY INTERRUPTS ARE GLOBALLY ENABLED 0=PHY INTERRUPTS ARE GLOBALLY ENABLED	R/W
6~0	RESERVED	WRITE AS 0, IGNORE ON READ	R/W

FIG. 14

BITS	NAME	DESCRIPTION	R/W
15	TxON	1=TxON SIGNAL IS ASSERTED 0=TxON SIGNAL IS NOT ASSERTED	R
14	BkON	1=BkON SIGNAL IS ASSERTED 0=BkON SIGNAL IS NOT ASSERTED	R
13	TxV1M1	1=TxV1M1 SIGNAL IS ASSERTED 0=TxV1M1 SIGNAL IS NOT ASSERTED	R
12	RxON	1=RxON SIGNAL IS ASSERTED 0=RxON SIGNAL IS NOT ASSERTED	R
11	CS	1=CS SIGNAL IS ASSERTED 0=CS SIGNAL IS NOT ASSERTED	R
10	CD	1=CD SIGNAL IS ASSERTED 0=CD SIGNAL IS NOT ASSERTED	R
9	RxV1M1	1=RxV1M1 SIGNAL IS ASSERTED 0=RxV1M1 SIGNAL IS NOT ASSERTED	R
8	RxErr	1=RxErr SIGNAL IS ASSERTED 0=RxErr SIGNAL IS NOT ASSERTED	R
7	INTERRUPT ENABLE	1=PHY INTERRUPTS ARE GLOBALLY ENABLED 0=PHY INTERRUPTS ARE GLOBALLY DISABLED	R
6~0	RESERVED	IGNORE ON READ	R

FIG. 15

BITS	NAME	DESCRIPTION	R/W
15	CS_ON ENABLE	1=ENABLE INTERRUPT WHEN CS SIGNAL BECOMES ASSERTED 0=DISABLE CS_ON INTERRUPT	R/W
14	CS_OFF ENABLE	1=ENABLE INTERRUPT WHEN CS SIGNAL BECOMES DE-ASSERTED 0=DISABLE CS_OFF INTERRUPT	R/W
13	CD_ON ENABLE	1=ENABLE INTERRUPT WHEN CD SIGNAL BECOMES ASSERTED 0=DISABLE CD_ON INTERRUPT	R/W
12	RxON_ON ENABLE	1=ENABLE INTERRUPT WHEN RxON SIGNAL BECOMES ASSERTED 0=DISABLE RxON_ON INTERRUPT	R/W
11	RxON_BkON ENABLE	1=ENABLE INTERRUPT WHEN RxON SIGNAL BECOMES ASSERTED DURING THE BACKOFF SLOTS 0=DISABLE RxON_BkON INTERRUPT	
10	RxErr_ON ENABLE	1=ENABLE INTERRUPT WHEN RxErr SIGNAL BECOMES ASSERTED 0=DISABLE RxErr_ON SIGNAL	R/W
9	PHY RxFifo OVERRUN ENABLE	1=ENABLE INTERRUPT WHEN PHY's RECEIVE FIFO OVERRUN 0=DISABLE THE INTERRUPT	R/W
8	PHY TxFifo UNDERRUN ENABLE	1=ENABLE INTERRUPT WHEN PHY's TRANSMIT FIFO IS UNDERRUN 0=DISABLE THE INTERRUPT	R/W
7	PHY SAMPLE DATA READY ENABLE	1=ENABLE INTERRUPT WHEN PHY's SAMPLE DATA IS READY FOR DSP PROCESSING 0=DISABLE THE INTERRUPT	R/W
6	PHY LOG DATA READY	1=ENABLE INTERRUPT WHEN PHY's LOG DATA IS READY FOR DSP/HOST TO SAMPLE 0=DISABLE THE INTERRUPT	R/W
5~0	RESERVED	INITIALIZED WITH 0 AND IGNORE ON READ	R/W

FIG. 16

BITS	NAME	DESCRIPTION	R/W
15	CS_ON	1=AN INTERRUPT OF CS SIGNAL BECOMES ASSERTED HAS BEEN GENERATED 0=CS_ON INTERRUPT IS NOT GENERATED	R
14	CS_OFF	1=AN INTERRUPT OF CS SIGNAL BECOMES ASSERTED HAS BEEN GENERATED 0=CS_OFF INTERRUPT IS NOT GENERATED	R
13	CD_ON	1=AN INTERRUPT OF CD SIGNAL BECOMES ASSERTED HAS BEEN GENERATED 0=CD_ON INTERRUPT IS NOT GENERATED	R
12	RxON_ON	1=AN INTERRUPT OF RxON_ON SIGNAL BECOMES ASSERTED HAS BEEN GENERATED 0=RxON_ON INTERRUPT IS NOT GENERATED	R
11	RxON_BkON	1=AN INTERRUPT OF RxON SIGNAL BECOMES ASSERTED DURING THE BACK OFF SLOTS HAS BEEN GENERATED 0=RxON_BkON INTERRUPT IS NOT GENERATED	R
10	RxErr_ON	1=AN INTERRUPT OF RxErr SIGNAL BECOMES ASSERTED HAS BEEN GENERATED 0=RxErr_ON INTERRUPT IS NOT GENERATED	R
9	PHY RxFifo OVERRUN	1=AN INTERRUPT OF PHY's RECEIVE FIFO OVERRUN HAS BEEN GENERATED 0=THIS INTERRUPT IS NOT GENERATED	R
8	PHY TxFifo UNDERRUN	1=AN INTERRUPT OF PHY's TRANSMIT FIFO IS UNDERRUN HAS BEEN GENERATED 0=THIS INTERRUPT IS NOT GENERATED	R
7	PHY SAMPLE DATA READY	1=AN INTERRUPT OF PHY's SAMPLE DATA IS READY FOR DSP PROCESSING HAS BEEN GENERATED 0=THIS INTERRUPT IS NOT GENERATED	R
6	PHY LOG DATA	1=AN INTERRUPT OF PHY's LOG DATA IS READY FOR DSP/HOST TO SAMPLE 0=THIS INTERRUPT IS NOT GENERATED	R
5~0	RESERVED	IGNORE ON READ	R

FIG. 17

BITS	NAME	DESCRIPTION	R/W
15	RESET	1=PHY RESET 0=NORMAL OPERATION	R/W
14	LOOPBACK	1=ENABLE LOOPBACK MODE 0=DISABLE LOOPBACK MODE	R/W
13	BAUDRATE SELECTION	1=4MBAUD SUPPORTED 0=4MBAUD NOT SUPPORTED	R/W
12,11	MODE SLECTION	00=2.0 MODE 01=1.0 MODE 10= COMPATIBILIY MODE 11=MODE AUTOMATIC SELECTION	R/W
10	COLLISION TEST	1=ENABLE CD SIGNAL TEST 0=DISABLE CD SIGNAL TEST	R/W
9	POWER MODE	1=LOW POWER STATE 0=NORMAL POWER STATE	R/W
8:0	RESERVED	WRITE AS 0, IGNORE ON READ	R/W

FIG. 18

BITS	NAME	DESCRIPTION	R/W
15	RESERVED	WRITE AS 0, IGNORE ON READ	R
14	LOOPBACK	1=PHY IS IN LOOPBACK MODE 0=PHY IS NOT IN LOOPBACK MODE	R
13	BAUDRATE SELECTION	1=PHY SUPPORTS 4MBAUD 0=PHY DOES NOT SUPPORT 4MBAUD	R
12,11	MODE STATUS	00=PHY IS IN 2.0 ONLY MODE 01=PHY 1.0 ONLY MODE 10=PHY IS IN COMPATIBILITY MODE 11=PHY IS IN AUTOMATIC SELECTION MODE	R
10	RESERVED	WRITE AS 0 IGNORE ON READ	R
9	POWER MODE	1=PHY IS IN LOW POWER STATE 0=PHY IS IN NORMAL POWER STATE	R
8:0	RESERVED	WRITE AS 0, IGNORE ON READ	R

FIG. 19

REGISTER INDEX	REGISTER NAME	DESCRIPTION	R/W	IMPLEMENTATION
0	TxFRAME LENGTH	BYTE COUNT OF FRAME TRANSMITTED FROM MAC TO PHY	PHY READ	PHY
1	RxFRAME LENGTH	BYTE COUNT OF FRAME TRANSMITTED FROM PHY TO MAC	PHY WRITE	PHY
2	SIGNAL CONTROL	MAC/PHY INTERFACE SIGNAL CONTROL REGISTER	PHY WRITE	PHY
3	SIGNAL STATUS	MAC/PHY SIGNALING STATUS	PHY READ	PHY
4	CRC32 HIGH REGISTER	CRC32 HIGH 16 BITS	PHY WRITE	PHY
5	CRC32 LOW REGISTER	CRC32 LOW 16 BITS	PHY WRITE	PHY
6	CRC16 REGISTER	CRC16	PHY WRITE	PHY
7	PHY MANAGEMENT CONTROL REGISTER	DESCRIBED IN 5.0	PHY READ	PHY
8	PHY MANAGEMENT STATUS REGISTER	DESCRIBED IN 5.0	PHY WRITE	PHY

FIG. 20

BITS	NAME	DESCRIPTION	R/W
15	RxON	1=SET RxON SIGNAL 0=CLEAR RxON SIGNAL	R/W
14	RxV1M1	1=SET RxV1M1 SIGNAL 0=CLEAR RxV1M1 SIGNAL	R/W
13	CS	1=SET CS SIGNAL 0=CLEAR RX SIGNAL	R/W
12	CD	1=SET CD SIGNAL 0=CLEAR CD SIGNAL	R/W
11	RxErr	1=SET RxErr SIGNAL 0=CLEAR RxErr SIGNAL	R/W
10~0	RESERVED	WRITE AS 0, IGNORE ON READ	R/W

FIG. 21

REGISTER INDEX	REGISTER NAME	DESCRIPTION	R/W	IMPLEMENTATION
0	SAMPLE DATA ADDRESS	SAMPLE DATA BUFFER START ADDRESS	DSP WRITE	DSP
1	SAMPLE DATA LENGTH	THE NUMBER OF DATA BYTES NEED TO BE TRANSFERRED FROM THE PHY	DSP WRITE	DSP
2	Rx SAMPLE DATA LENGTH	THE NUMBER OF DATA WORDS (16 BIT) ACTUALLY TRANSFERRED FROM THE PHY	DSP READ	PHY
3	DSP DATA LENGTH	THE NUMBER OF DATA WORDS (16 BIT) ACTUALLY TRANSFERRED FROM THE PHY	DSP WRITE	DSP
4	DSP DATA PORT	DSP DATA OUTPUT PORT	DSP WRITE	DSP

FIG. 22

REGISTER INDEX	REGISTER NAME	DESCRIPTION	R/W	IMPLEMENTATION
0	Rx SAMPLE DATA LENGTH	THE NUMBER OF DATA WORDS (16 BIT) ACTUALLY TRANSFERRED FROM THE PHY TO THE DSP	PHY WRITE	PHY
1	DSP DATA LENGTH	THE NUMBER OF DATA BYTES NEEDED TO BE TRANSFERRED TO THE PHY	PHY READ	DSP
2	DSP DATA PORT	DSP DATA INPUT PORT	PHY READ	PHY

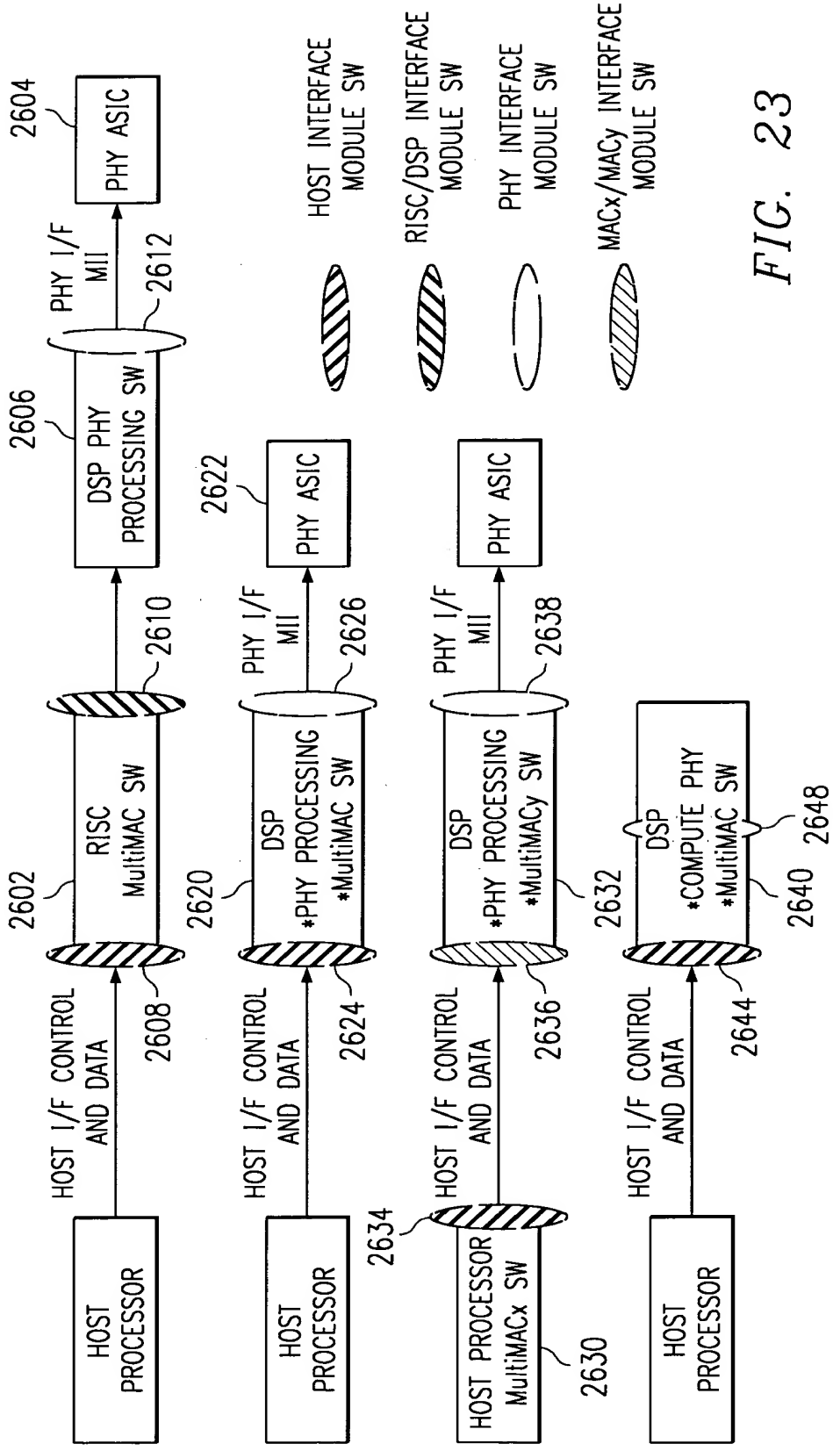

FIG. 23

FIG. 24